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Published in:
Advanced materials

DOI:
10.1002/adma.201701764

Publication date:
2017

An All-Solution-Based Hybrid CMOS-Like Quantum Dot/Carbon Nanotube Inverter

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The development of low-cost, flexible electronic devices is subordinated to the advancement in solution-based and low-temperature-processable semiconducting materials, such as colloidal quantum dots (QDs) and single-walled carbon nanotubes (SWCNTs). Here, excellent compatibility of QDs and SWCNTs as a complementary pair of semiconducting materials for fabrication of high-performance complementary metal-oxide-semiconductor (CMOS)-like inverters is demonstrated. The n-type field effect transistors (FETs) based on I^- capped PbS QDs (V_{th} = 0.2 V, on/off = 10^5, $S_{S\text{-}th}$ = 114 mV dec^{-1}, μ_e = 0.22 cm^2 V^{-1} s^{-1}) and the p-type FETs with tailored parameters based on low-density random network of SWCNTs (V_{th} = –0.2 V, on/off > 10^5, $S_{S\text{-}th}$ = 63 mV dec^{-1}, μ_h = 0.04 cm^2 V^{-1} s^{-1}) are integrated on the same substrate in order to obtain high-performance hybrid inverters. The inverters operate in the sub-1 V range (0.9 V) and have high gain (76 V/V), large maximum-equal-criteria noise margins (80%), and peak power consumption of 3 nW, in combination with low hysteresis (10 mV).

Solution-processable electronic materials are in great demand since they can be applied in low-cost, flexible electronic devices and circuits. Among the materials, which have attracted the most attention, are single-walled carbon nanotubes (SWCNTs) and colloidal quantum dots (QDs).

Over the last few years, QDs have been used to fabricate solar cells, LEDs, displays, near-infrared photodetectors, and microelectronic circuits.[1–10] PbS and CdSe QDs have been the most studied; however, their applicability in electronics is hampered by the difficulty in achieving unipolar p-type charge transport and high device stability. On the other hand, SWCNTs have been implemented in radio frequency identification tags, sensors, memories, and digital circuits.[11–17] In its turn, the continuous, stable, and reliable n-type doping of SWCNTs still remains challenging, limiting the performance of SWCNT-based electronics.

Both CdSe QDs (as n-type material) and SWCNTs (as p-type material) field effect transistors (FETs) were reported as building blocks of unipolar logic devices (e.g., inverters).[8,10,18,19] The unipolar logic in theory features lower noise margin (i.e., a figure of merit of the stability of the logic circuit to a voltage noise) and higher power consumption with respect to ambipolar (or complementary metal-oxide-semiconductor (CMOS)-like) logic devices.[20,21] As a possible improvement, ambipolar inverters based on PbS QDs or nanocubes FETs were reported.[9,22] However, the low bandgap in ambipolar, often partially sintered PbS QDs films results in an high "off" current of the transistors, hereby increasing the power consumption and affecting the noise margins of the inverter. SWCNTs, similarly, have been utilized in doping-free ambipolar inverters.[23–25] Various strategies have been applied to obtain n-doped SWCNTs for the fabrication of (CMOS)-like inverters.[26–31] Since reliable, stable, and tunable n-doping of SWCNTs still remains challenging, hybrid inverters, which combine complementary pair of semiconductors as SWCNTs with an n-type material, such as MoS_2, IGZO, IZO, or ZTO, have been reported.[32–36] Although the reported inverters operate successfully, their performance in terms of noise margins and power consumption leaves much to be desired.

In the case of the QDs, to the best of our knowledge, the hybrid approach for the fabrication of CMOS-like inverters was not attempted yet. Stable, solution-based, unipolar FETs with well-controlled threshold voltage, low hysteresis, and high mobility are in high demand for fabrication of high-noise margins, low-voltage, and low-power-consumption inverters and other logic elements.

Here, we report a hybrid CMOS-like inverter, integrated on a single glass substrate, based on all-solution-based FETs gated with a high capacitance (157 nF cm^{-2}) P(VDF-TrFE-CFE)/PMMA polymer dielectric layer. The n-type FETs are made of I^- capped PbS QDs and show an on-off ratio of 10^5, a subthreshold swing of 114 mV dec^{-1}, a threshold voltage of 0.2 V, a

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DOI: 10.1002/adma.201701764

hysteresis of 20 mV, and electron mobility of 0.22 $cm^2\ V^{-1}\ s^{-1}$. The p-type transistor is based on a low-density random network of polymer selected semiconducting SWCNTs and features an on-off ratio of 10^5, a subthreshold swing of 63 mV dec^{-1}, a threshold voltage of −0.2 V, a hysteresis of 20 mV, and a linear mobility of 0.04 $cm^2\ V^{-1}\ s^{-1}$. The CMOS-like inverter operates in sub-1 V voltage range (power supply voltage of 0.9 V) and shows high static gain (76 V/V), large noise margins (80%), and small hysteresis (10 mV), with the peak power consumption of 3.5 nW, which are the best reported values for all-solution-processable inverters to date.

As it was reported earlier, P(VDF-TrFE-CFE) is a good gate dielectric material for solution-processable FETs based on SWCNTs, QDs, and organic semiconductors.[37–39] Since P(VDF-TrFE-CFE) does not contain electron trapping groups and can encapsulate the active layer, protecting it from water and oxygen, this polymer is especially interesting as a gate material for n-type FETs. However, when P(VDF-TrFE-CFE) is used as gate dielectric several challenges appear as the difficulty to obtain continuous and smooth layers and the hysteresis loop in the transfer curves, which can be explained by its relaxor ferroelectric nature.[38] To decrease the hysteresis and increase the reproducibility of the device fabrication, in this work we used on top of the P(VDF-TrFE-CFE) film a thin film of amorphous poly(methyl methacrylate) (PMMA). PMMA is a low-dielectric-constant "passive" layer in series with the relaxor ferroelectric P(VDF-TrFE-CFE), thus the addition of the PMMA reduces the ferroelectric properties and the dielectric constant of the combined dielectric layer (Figure S1, Supporting Information).[40]

First, the difference between P(VDF-TrFE-CFE)-only and P(VDF-TrFE-CFE)/PMMA as gate dielectric layers in I^- capped PbS QDs FETs is investigated, the device structure used is displayed schematically in **Figure 1**A. Almost pure n-type charge transport in the PbS QDs transistor is achieved, as it is demonstrated by the output curves shown in Figure 1B. This is obtained using a low-work-function metal, such as Ag, for the fabrication of source and drain electrodes, lithographically patterned on n^{++} Si/SiO_2 substrate, that blocks holes and favors electron injection. Before deposition of the active material, the substrate is annealed in an N_2-filled glovebox in order to desorb oxygen and water from the SiO_2 surface. After depositing the I^- capped PbS QDs film, the P(VDF-TrFE-CFE) or P(VDF-TrFE-CFE)/PMMA top gate was spin-coated, as schematically indicated in Figure 1A.

The electron saturation current measured for the same gate voltage is higher for P(VDF-TrFE-CFE) -gated devices than for the P(VDF-TrFE-CFE)/PMMA-gated ones, due to higher gate capacitance of the first (204 nF cm^{-2} ($k = 46$)) with respect to the second gate (157 nF cm^{-2} ($k = 35$)). It is also important to note that the two types of transistors exhibit different shifts of the threshold voltage due to the different ferroelectric properties of the two gates. The small hysteresis in the output curves displayed in Figure 1B (the dashed curves show the reverse voltage sweep) indicates a low charge trapping rate in the film and at the interfaces, which is a nontrivial achievement in quantum dot FETs. The different hysteresis shape indicates dissimilar underlying processes in P(VDF-TrFE-CFE) and P(VDF-TrFE-CFE)/PMMA-gated FETs; in case of P(VDF-TrFE-CFE)/PMMA, the reverse sweep current is lower than the forward sweep

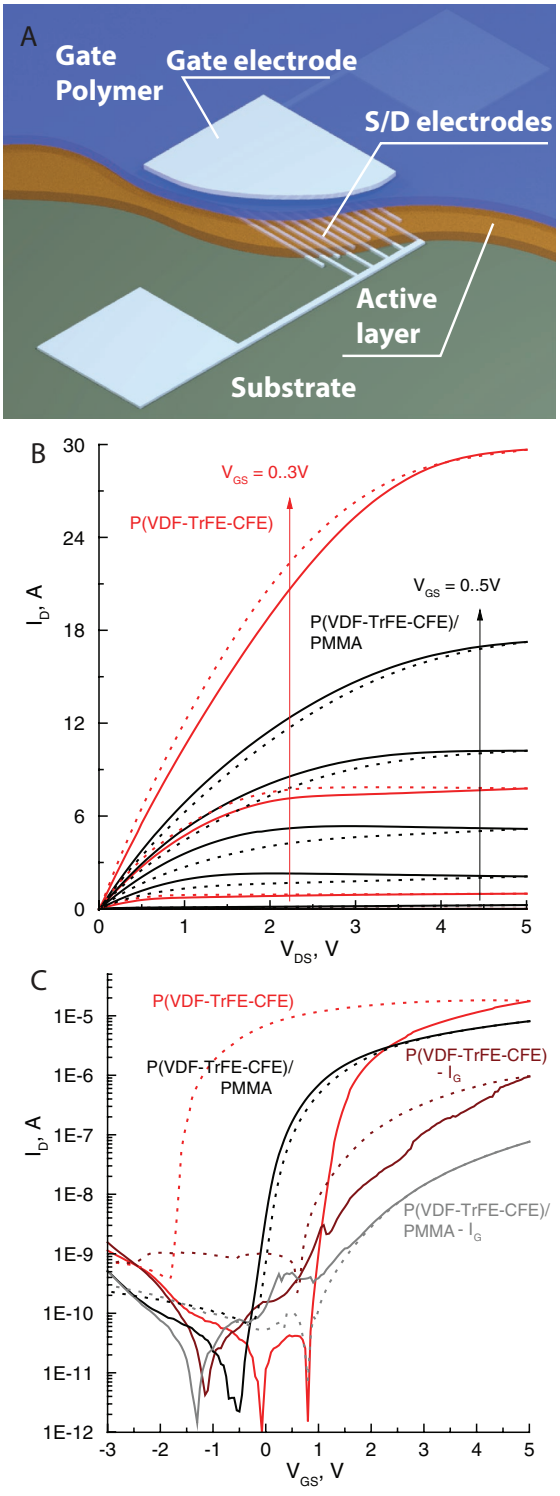

Figure 1. Comparison of P(VDF-TrFE-CFE)/PMMA and P(VDF-TrFE-CFE) as gate dielectrics for I^- capped PbS QDs FETs. A) Schematic structure of the device. B) Comparison of the output characteristics of I^- capped FETs with P(VDF-TrFE-CFE) (V_{GS} = 0.3 V, ΔV_{GS} = 1 V) and P(VDF-TrFE-CFE)/PMMA (V_{GS} = 0.5 V, ΔV_{GS} = 1 V). The arrows indicate increasing of V_{GS}. C) Comparison of the transfer characteristics of I^- capped FETs with P(VDF-TrFE-CFE) and P(VDF-TrFE-CFE)/PMMA (V_{DS} = 1 V) gate dielectrics with corresponding gate leakages. Dotted curves represent the reverse hysteresis branches.

because of charge trapping, probably caused by defects formed at the QD surface during the ligand-exchange process, which is a frequently reported mechanism in PbS QDs FETs. In case of P(VDF-TrFE-CFE), the reverse current is higher, most probably because of the remnant polarization of the gate dielectric in the region close to the source/drain electrodes due to the polarization of the gate electrode across the channel that overcomes the current decrease due to the charge-trapping process. This effect is even more visible in the transfer curves (Figure 1C). The sweep of the gate voltage polarizes the gate and the difference in the remnant polarization causes strong differences in the hysteresis magnitude and shape. For P(VDF-TrFE-CFE)/PMMA, the hysteresis is only 0.17 V, which to the best of our knowledge, is the smallest reported value for PbS QDs FETs; for P(VDF-TrFE-CFE) the hysteresis is significantly larger (2.7 V) and the reverse current is higher than the forward one, showing a similar behavior as in the output curves. Because of the relaxor ferroelectric nature of P(VDF-TrFE-CFE), the remnant polarization is not stable and decays within minutes resulting in a decay of the drain current after applying a gate voltage pulse to the FET (Figure S2, Supporting Information). Although the gate leakage current for P(VDF-TrFE-CFE) (dark red curve in Figure 1) is almost one order of magnitude higher than the leakage through P(VDF-TrFE-CFE)/PMMA (gray curve in Figure 1), the gate leakages vary for FETs and over multiple devices providing no strong evidence that the P(VDF-TrFE-CFE)/PMMA insulates the gate electrode better than the P(VDF-TrFE-CFE). In the device configuration used in this work, the gate electrode is not patterned and the overlap of the gate and source/drain electrodes is quite high, thus increasing the possibility of a defect leading to a direct leakage from the gate to the source or drain electrodes. Additionally, the contact probes can easily penetrate the gate electrode metal and the gate dielectric, during the measurement of the devices, causing a current leakage through the active layer, proportional to the applied source/gate voltage difference. Here, it is also important to notice that the P(VDF-TrFE-CFE)/PMMA gate encapsulates the active layer making these devices stable for several months in an N_2-filled glovebox and for several hour exposure to air, with no clear change in the threshold voltage, electron mobility, or on-off ratio.

Figure 2 shows the complementary pair of FETs integrated on the single glass substrate. After cleaning and annealing the glass substrate similarly to the Si/SiO_2 substrate described above, the PbS QDs film was spin-coated onto one part of the substrate and the SWCNTs random network was deposited, using a blade-coating technique, on the opposite part. The morphology of the two layers is shown by the atomic force microscopy (AFM) images reported in Figure 2A. Subsequently, the P(VDF-TrFE-CFE) and PMMA polymer layers were spin-casted on the whole substrate and the gate electrodes were evaporated through a shadow mask. Figure 2 B,C shows output and transfer curves of the SWCNTs FET (left) and the PbS QDs FET (right), respectively. The channel geometries were selected to achieve a complementary pair of FETs with appropriate threshold voltages and linear/saturation current. The linear and the saturation electron mobilities of the PbS QDs film, extracted from V_{DS} = 1 V and V_{DS} = 5 V transfer curve for the FET with the channel length of 30 µm and the channel width of 5 mm (Figures S4 and S5

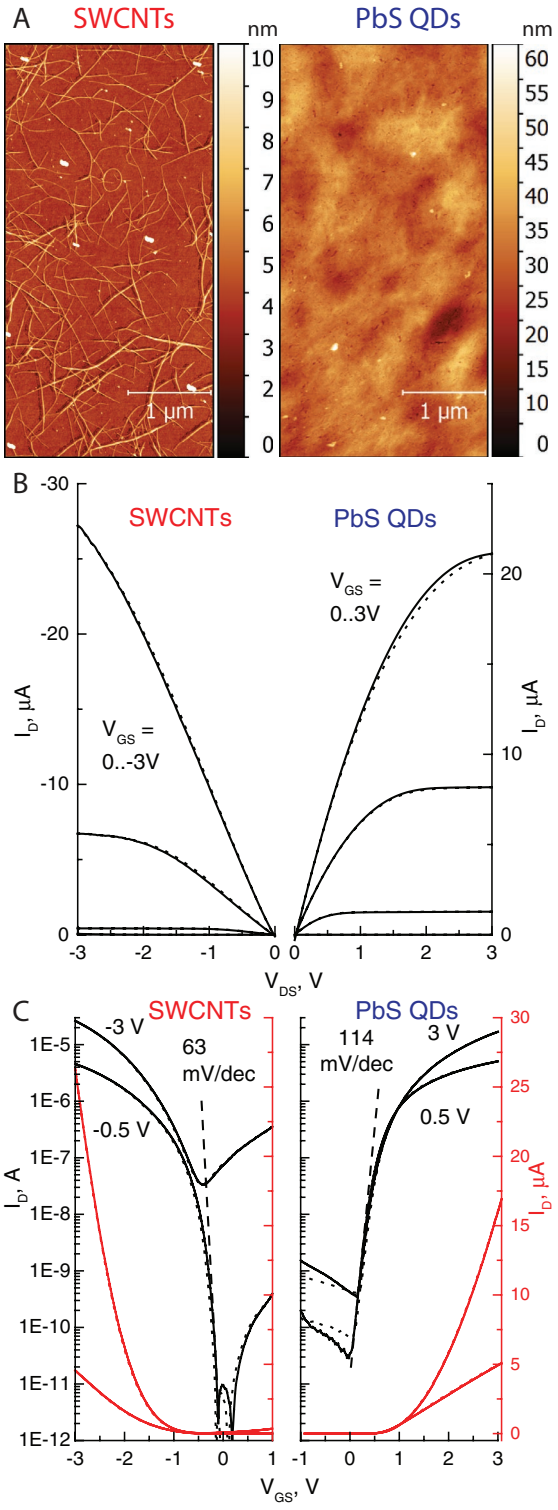

Figure 2. Complementary SWCNTs and I^- capped PbS QDs FETs with the P(VDF-TrFE-CFE)/PMMA gate dielectric integrated on a glass substrate. A) AFM images of SWCNTs random network and PbS QDs thin film (120 nm). B) Output characteristics of SWCNT (left) and I^- capped PbS QDs (right) FETs. C) Transfer curves of SWCNTs (left) and I^- capped PbS QDs (right) FETs in logarithmic (black) and linear (red) scale for V_{DS} = 0.5 V (linear regime) and 3 V (saturation regime). The dashed lines indicate subthreshold swing; dotted curves are reverse hysteresis branches.

and Table S1, Supporting Information), have values of about 0.22 cm^2 V^{-1} s^{-1}. Furthermore, the contact-resistance correction obtained by analyzing transistors with channel lengths 5, 10, 20, 30, and 40 µm confirms the above linear mobility value (Table S2, Supporting Information). This electron mobility, in combination with the low hysteresis, the subthreshold swing of 114 mV dec^{-1}, the on-off ratio of 10^5, and the threshold voltage of 0.2 V, characterizes the P(VDF-TrFE-CFE)/PMMA-gated PbS QDs FETs as a suitable n-type component for low-cost and low-voltage electronics. The off current is limited by the intrinsic ambipolarity and relatively low bandgap of PbS QDs explaining the minor injection of holes in the channel even from the low-work-function electrodes. The optical absorbance measurements (Figure S3, Supporting Information) show that the ligand exchange and annealing do not cause significant sintering of I^- capped PbS QDs film; therefore, the quantum confinement of the individual quantum dots is not compromised enabling high on-off ratio and low subthreshold swing.

As mentioned, a low-density semiconducting SWCNTs random network (see the AFM image in Figure 2A, left) was deposited since the hole mobility of a high-density network can be orders of magnitude higher than the electron mobility of PbS QDs.[41] Additionally, increasing the number of intertube crossings in the current pathway can be considered as a contact resistance that increases with the channel length.[42] Therefore, the correction of the mobility for the channel-length-independent contact resistance, made for PbS QDs film, cannot be implemented for the SWCNTs low-density random network. Additionally, using the geometrical size of the channel in the calculations leads to the underestimation of the mobility: the actual channel width for the current pathway is strongly overestimated since the current pathway takes place through individual carbon nanotubes and not through the geometrical channel width; the actual channel length is underestimated, since the current pathway goes through interconnected carbon nanotubes, which is significantly larger than the direct distance between the patterned electrodes. Without any corrections, the linear and the saturation hole mobility extracted for the device with 10 µm channel, presented in Figure 2, are 0.04 and 0.09 cm^2 V^{-1} s^{-1}, respectively. The value of linear hole mobility is more than twice lower than the saturation mobility enforcing our assumption that the linear current has been influenced by the contact resistance. A minor electron current is observed in the transfer curves because of intrinsic nature of SWCNTs purified with the polyfluorene derivative poly(9,9-di-*n*-dodecylfluorenyl-2,7-diyl) (PF-12) polymer, which for higher source–drain voltages affects the off-state of the FET.[43] However, for low-voltage operation (V_{DS} = 0.5 V), the device showed an on-off ratio higher than 10^5, very low subthreshold swing of 63 mV dec^{-1} (which is only slightly higher than the theoretical limit of 60 mV dec^{-1} for 300 K), and a threshold voltage of –0.2 V.

Figure 3 shows the performance of the CMOS-like inverter based on P(VDF-TrFE-CFE)/PMMA gated p-type SWCNTs and n-type PbS QDs FETs. The inverter was characterized using four probes, connecting the complementary pair of FETs to the measuring setup according to the schematics in the inset of Figure 3A. The voltage transfer curve (VTC) of the inverter, operating for V_{DD} = 0.9V, is shown in Figure 3A for the forward (solid black curve) and reverse (dashed black curve) sweep.

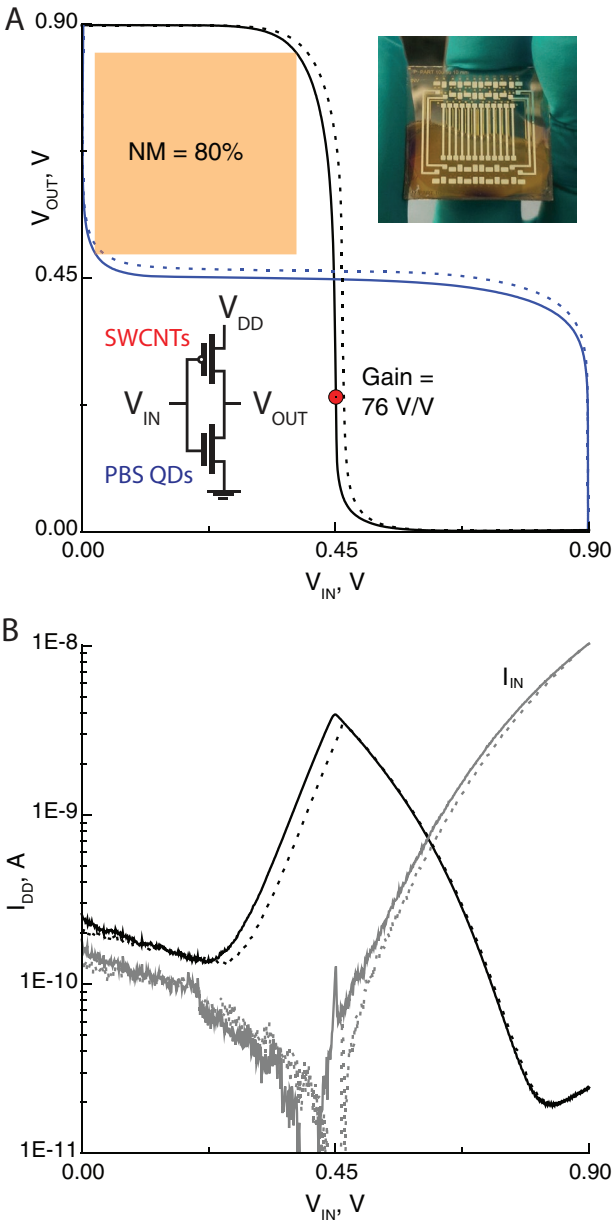

Figure 3. Hybrid CMOS-like PbS QDs/SWCNTs inverter. A) The direct (black) and mirrored (blue) VTC of the inverter for V_{DD} = 0.9 V. Inset: Photograph of the substrate and schematic connection of the inverter. The orange square indicates static noise margins determined according to the maximum equal criteria principle. B) The current through the V_{DD} terminal (black) with indication of the current through the V_{IN} terminal (gray). Dotted curves are the reverse hysteresis branches.

The static gain reaches a maximum value of 76 V/V for V_{IN} = 0.45 V. For the high-output state of the inverter (V_{IN} = 0 V), the output voltage is 99.77% of V_{DD}, and for low-output state (V_{IN} = 0.9 V), it is 0.31% of V_{DD}. The mirrored VTC (blue solid and dashed lines for forward and reverse hysteresis, respectively) is shown in order to illustrate the noise margins of 80%, determined accordingly to the "maximum equal criteria" principle for the forward sweep curve.[21,44] The current, measured through the power supply (black curve, I_{DD}) and input

(gray curve, I_{IN}) terminals are plotted in Figure 3B. The VTC hysteresis of 10 mV is caused by the PbS QDs FET, which follows from the hysteresis shape of the current measurements. The I_{DD} is 0.2 nA (in the high-output state) and 25 pA (in the low-output state), which are limited, respectively, by the gate leakage current in the PbS QDs FET and by the minor electron current through the SWCNTs FET. The I_{IN} is determined by the gate leakages and is ≈0.1 nA for high-output state (gate leakage through the SWCNTs FET) and is growing up to 10 nA for low-output state (gate leakage through the PbS QDs FET). The maximum power consumption of the inverter occurs in the switching point and is 3 nW. Therefore, to the best of our knowledge, this hybrid inverter shows the highest reported static gain and noise margins for transistors made with fully solution-processable materials.

As for reproducibility of our results, since the mobility of SWCNTs random network depends strongly on the density, the switching voltage (the noise margins) and the gain value varied slightly for different samples. FETs made from high-density SWCNTs network showed hole mobility of 0.9 $cm^2\ V^{-1}\ s^{-1}$; however, the gate leakage current increased proportionally and influenced the VTC curves of the inverters. Although the inverters showed high performance with the noise margins up to 84% (for V_{DD} = 2 V) and the gain up to 220 V/V (for V_{DD} = 3 V), the steady-state power consumption increased because of the gate leakage and electron current for higher power supply voltages in the SWCNTs FETs (Figure S6, Supporting Information).

In conclusion, we show that PbS QDs film and SWCNTs random network can be used as a complementary pair of materials for fabrication of high-performance all-solution-processable CMOS-like inverters, build up from high-*k*-polymer-gated FETs. The n-type FET shows on-off ratio of 10^5, a subthreshold swing of 114 mV dec^{-1}, a threshold voltage of 0.2 V, a hysteresis of 20 mV, and electron mobility of 0.22 $cm^2\ V^{-1}\ s^{-1}$. Silver electrodes in combination with I^- ligands determine an almost perfect unipolar n-type charge transport through PbS QDs film. A low-density network of SWCNTs was used in order to get complementary charge transfer characteristics to the n-type PbS QDs FET. The p-type SWCNTs FETs display an on-off ratio higher than 10^6, a subthreshold swing of 63 mV dec^{-1}, a threshold voltage of −0.2 V, a hysteresis of 20 mV, and a linear mobility of 0.04 $cm^2\ V^{-1}\ s^{-1}$. The reported inverter features sub-1 V operation (V_{DD} = 0.9 V) with the highest reported static gain (76 V/V) and noise margins (80%) for fully solution-processable devices, to the best of our knowledge. It should be noted that the high-*k* gate dielectric P(VDF-TrFE-CFE)/PMMA (k = 35) can be used in low-voltage, low-hysteresis FETs providing a gate capacitance of 157 nF cm^{-2} and also serves as an encapsulating layer for air-sensitive materials.

As future perspective, ample room is available for further improving the performance, reproducibility, and fabrication process of these inverters. First, using a patterned gate electrode would improve the frequency response of the logic device. Second, recent developments in PbS QDs inks based on solution-phase ligand exchange may allow switching to a single-step printing technique, for which SWCNTs have been demonstrated to be fully compatible.[25,45,46] Furthermore, a robust self-assembly of SWCNTs was recently reported in FETs, a technique that could be used for the fabrication of integrated inverters with SWCNTs and PbS QDs.[47]

Experimental Section

PbS QDs Synthesis: Materials: Lead (II) acetate trihydrate ($Pb(CH_3COO)_2 \cdot 3H_2O$, ≥99.99%, Aldrich), bis(trimethylsilyl)sulfide (TMS_2S, Aldrich), 1-octadecene (ODE, 90%, Aldrich), oleic acid (OA, 90%, Aldrich), ethanol (Fluka), hexane (Aldrich), and tetrachloroethylene (TCE, 99%, Aldrich) were used as received.

3.2 nm PbS QDs were synthesized according to the method of Hines and Scholes with slight modifications.[48] $Pb(CH_3COO)_2 \cdot 3H_2O$ (1.5 g, 4 mmol), ODE (47.2 mL), and oleic acid (2.8 mL) were mixed in a three-neck flask. The mixture was degassed under vacuum at 120 °C for 1 h. Then temperature was adjusted to 95 °C under argon flow. The heating mantle was removed and solution of TMS_2S (0.42 mL, 2 mmol) in 10 mL ODE (dried) was injected into vigorously stirring lead oleate solution. After 5 min, the reaction mixture was cooled down to room temperature by ice bath. QDs were washed three times with toluene/ethanol solvent/nonsolvent pair (first washing: 30 mL hexane/120 mL ethanol; second washing: 30/36; third washing: 15/16), redissolved in 7 mL hexane and filtered through 0.2 µm PTFE filter.

Preparation and Characterization of Semiconducting SWNTs Dispersion: HiPco SWCNTs (0.8-1.2 nm) purchased from Unidym Inc. were used as received. The polymer PF-12 was solubilized in toluene using a high-power ultrasonicator (Misonix 3000) with cup horn bath (output power 69 W) for 20 min. Subsequently, SWCNTs were added to form the SWCNT:polymer dispersions with a weight ratio of 1:2 (3 mg of SWNTs, 6 mg of polymer, 15 mL of toluene). These solutions were then sonicated for 2 h at 69 W and 16 °C.

After ultrasonication, the dispersions were centrifuged at 30 000 rpm (109 000 g) for 1 h in an ultracentrifuge (Beckman Coulter Optima XE-90; rotor: SW55Ti) to remove all the remaining nanotube bundles and heavy-weight impurities. After the centrifugation, the highest density components precipitate at the bottom of the centrifugation tube, while the low-density components, including small bundles and individualized SWNTs wrapped by the polymer, and free polymer chains, stay in the upper part as supernatant.

One extra step of ultracentrifugation was implemented to decrease the amount of free polymer in solution (enrichment).[49] For this purpose, the supernatant obtained after the first ultracentrifugation was centrifuged for 5 h at 55 000 rpm (367 000 g). The individualized SWNTs were then precipitated to form a pellet and the free polymer was kept in the supernatant. Finally, the pellet was re-dispersed by sonication in toluene.

Substrate Preparation: Glass (for the inverters) or n^{++} Si/SiO_2 (for P(VDF-TrFE-CFE) and P(VDF-TrFE-CFE)/PMMA gate dielectrics comparison) substrates with lithographically patterned silver electrodes were cleaned, after lift-off of the photoresist, with light scrubbing with soap by a latex glove, rinsing and sonication in water, argon plasma treatment, sonication in acetone and, subsequently, isopropanol. Then the substrates were annealed in an N_2-filled glovebox before the deposition of the active layer.

Deposition of I^- Capped PbS QDs Film: The PbS QDs film was deposited by layer-by-layer spin-coating. To obtain dense, crack-free film, the first layer was deposited from 2 mg mL^{-1} solution of OA-capped PbS QDs in hexane, the next two layers from 20 mg mL^{-1} solution at a rate of 1000 rpm with an acceleration of 1000 rpm s^{-1}.[38] For inverters, only half of the substrate (size of 3 × 3 cm) was covered with the PbS QDs solution and the acceleration rate was kept to 500 rpm s^{-1} in order to prevent solution from spreading over the whole substrate during deposition. The ligand exchange was performed after deposition of each PbS QDs layer by covering the substrate with 30×10^{-3} M solution of tetrabutylammonium iodide (TBAI) in methanol and a subsequent double washing step using clean methanol. After each spin-coating/ligand-exchange step the substrate was dried for 15 s on a hotplate at 100 °C. After finishing, the substrate was annealed on a hotplate for

20 min at 120 °C. All the steps were performed in an oxygen and water-free (O_2 < 0.6 ppm, H_2O < 0.1 ppm) N_2-filled glovebox.

Deposition of SWCNT Film: Semiconducting SWCNTs were selected by polymer wrapping using the polyfluorene derivative PF-12 in toluene using the previously reported method briefly described below.[43] The SWCNTs film was deposited using a blade-coating technique inside N_2-filled glovebox. The substrate with previously deposited PbS QDs film covering half of the substrate was placed on a heated (55 °C) surface. 40 µL of a dispersion of SWCNTs (0.5 mg mL^{-1}) were dropped in the middle of the substrate, and excess of the solution was removed by a blade, located on 30 µm distance above the surface of the substrate and moving with the velocity of 5 mm s^{-1}. The direction of the blade is chosen in a way to deposit the SWCNTs random network on the half of the substrate free from the PbS QDs film. After completing the deposition of both materials, the substrate was annealed for 20 min on a hotplate (120 °C) inside the glovebox.

Deposition of P(VDF-TrFE-CFE) and P(VDF-TrFE-CFE) /PMMA: The P(VDF-TrFE-CFE) thin film (≈200 nm) was fabricated from a 50 mg mL^{-1} P(VDF-TrFE-CFE), VDF:TrFE:CFE = 62.6:29.4:8 solution in cyclohexanone via a two-step spin-coating process. First with the closed spin-coater lid at 1400 rpm, with an acceleration of 1000 rpm s^{-1} for 90 s, followed by an open lid step at 1000 rpm with an acceleration of 1000 rpm s^{-1} for 45 s. The substrate was then annealed at 120 °C for 20 min to dry the residual cyclohexanone.

For P(VDF-TrFE-CFE)/PMMA film, the PMMA film (≈10 nm) was spin-coated (closed lid: 3000 rpm, 3000 rpm s^{-1}, 20 s) on top of P(VDF-TrFE-CFE) from a 6 mg mL^{-1} PMMA solution in chloroform.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors would like to thank Arjen Kamp, Udo Douma, Johan Holstein, Martijn de Roosz, and Teodor Zaharia for technical help and assistance. The authors are grateful to Arnoud Everhardt for valuable discussions and help in ferroelectric characterization of polymer gate dielectrics. The Groningen team acknowledges the financial support of the European Research Council (ERC) starting grant (No. 306983) "Hybrid solution processable materials for optoelectronic devices" (ERC-HySPOD). M.V.K. acknowledges the financial support from the European Union through the FP7 (ERC Starting Grant NANOSOLID, GA No. 306733).

Conflict of Interest

The authors declare no conflict of interest.

Keywords

carbon nanotubes, colloidal quantum dots, field effect transistors, hybrid inverters

Received: March 29, 2017
Revised: May 15, 2017
Published online: July 17, 2017

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